IEEE AICAS 2025 Grand Challenge - LLM-Based Analog Circuit Design Competition

I. Track Overview

This competition track requires deploying and running large models on the hardware infrastructure of the Arm cloud platform. Using the Armv9 architecture CPU processor (T-Head Yitian 710) as the computing platform, participants will conduct analog circuit design automated with the Qwen large language model.

II. Background

Recent advancements in Large Language Models (LLMs) have unlocked transformative potential across numerous domains such as electronic design automation (EDA). LLM-driven solutions have demonstrated remarkable potential in digital circuit design, which promote AI-driven solutions evolving from circuit optimization to design automation. However, analog circuit design presents unique challenges due to its inherently complex, non-linear characteristics and strict precision requirements. LLM-driven analog circuit design is still in the exploratory stage.

The **AICAS2025 Challenge** seeks to accelerate the integration of LLMs into analog circuit design workflows, advancing the state-of-the-art in this field. Analog circuit design, a cornerstone of electronic systems, traditionally relies on skilled engineers performing manual, iterative design procedure that are time-intensive and error-prone. By leveraging LLMs, this competition aims to significantly reduce design cycles, enhance accuracy, and address the limitations due to conventional design methodologies, opening new opportunities for intelligent and automated design paradigms.

III. Competition Overview

A. Challenge Plan:

Participants must design and build AI agents for designing analog circuit via the **Qwen2.5 series** of large models. The goal is to autonomously complete the design of transistor-level operational amplifier circuits using the **SkyWater SKY130 PDK** open-source process design kit, ensuring the satisfaction of performance specifications (detailed information is in the evaluation section). The submitted designs will be scored

based on the performance of the generated circuits.

Qwen2.5 series large language models are developed by Alibaba with outstanding capabilities by optimizing architecture and inferencing efficiency to support applications like text generation, question answering, and dialogue systems. Additionally, **Qwen2.5** LLMs supports multimodal processing capability to handle both text and image data, enhancing its flexibility and application range. Users are allowed to configure **Qwen2.5** with different model scale settings to balance performance and resource requirements. The model's continuous learning ability ensures its adaptability to new tasks and data in dynamic environments.

The competition track is divided into two stages: a preliminary round and a final round. For both stages, participants are required to use the **Qwen2.5 series** (7B or below model parameters) to build intelligent agents. During **the preliminary round**, no specific hardware platform is provided, and each team can freely select a hardware platform to design, deploy, and optimize their intelligent agents. Participants must generate corresponding SPICE netlists according to given performance metrics and submit them for evaluation. For the preliminary round, **16 teams** would be selected to the final stage by their scores after code review. Additionally, **the top 10 teams** from the preliminary round will be invited to participate in an offline workshop. In **the final round**, all teams will use the cloud computing platform provided by the organizing committee, which is based on the **Armv9 architecture CPU processor (T-Head Yitian 710)**, to deploy intelligent agents for large-scale analog circuit models. Participants are required to generate circuit netlists to meet more performance specifications. Automated testing scripts will be used to evaluate the submissions for all teams. Based on the final rankings, the top three teams will be awarded and invited to the AICAS 2025 conference for the final defense.

B. Competition schedule:

- Preliminary Round Start: December 1, 2024
- Preliminary Round End: February 15, 2025
- Competition Workshop*: February 22, 2025
- Final Round Start: February 24, 2025
- Final Round End: March 24, 2025
- Deadline for code and technical report submission: March 30, 2025
- Results Announcement: April 10, 2025

- AICAS Conference & Ceremony**: April 28, 2025

Competition Workshop*: After the preliminary round, the organizing committee will host a competition workshop domestically, inviting the 10 shortlisted teams from the preliminary round to participate. The workshop will feature keynote speeches by experts from the organizing body and include networking activities. The committee will reimburse travel and accommodation expenses incurred by the participating teams for attending the workshop (subject to competition reward standards).

AICAS Conference & Ceremony**: After the final round, the organizing committee will invite the top three winning teams to the main venue of AICAS 2025 in Bordeaux, France, to present their work and participate in conference activities. The committee will reimburse travel and accommodation expenses incurred by the participating teams for attending the conference (subject to competition reward standards).

C. Registration for the AICAS Grand Challenge 2025 :

- Log in to the Tianchi platform at the provided URL: https://tianchi.aliyun.com/competition/entrance/532287/information?lang=en-us
- Complete the registration procedure. Participants are required to provide real-name verification.
- Each participating team can have up to five contestants and two supervisors, and each contestant can only participate in one team.
- The deadline for player registration, team change and other operations is 23:59:59, February 15, 2025. (**Verification Process：Tianchi official website -个人中心-认证-支付宝实名认证**).
- Scan the QR-Code and enter the Q&A group (Optional).
- This competition is open to students and researchers currently enrolled or affiliated with universities and research institutions.
- The staffs from T-head, Arm, Arm China and Institute for Intelligent Computing of Alibaba Group are not allowed to participate in the award evaluation.

D. Awards:

The total prize pool includes **$5,550** in cash prizes and **$7,500** in travel subsidies.

The top 16 teams from the preliminary round can advance to the final round, and the top 10 teams will be invited to the technical workshop in Hangzhou. The top 3 teams in the final round will be invited to the AICAS 2025 conference, and the organizing committee will provide travel subsidies as follows:

- **Hangzhou Technical Workshop**: USD 300 or CNY 2,100 (10 teams).
- **AICAS 2025**: USD 1,500 or CNY 10,500 (3 teams).

The selection of winners will be based on their final scores, submitted technical reports, and paper quality. The top 10 teams will receive cash prizes.

The distribution of pre-tax prizes is as follows:

- First Place: USD 2000 or CNY 14000 (for 1 team, ranking #1)
- Second Place: USD 1500 or CNY 10500 (for 1 teams, ranking #2)
- Third Place: USD 1,000 or CNY 7000 (for 1 teams, ranking #3)
- Award of Excellence: USD 150 or CNY 1050 (for 7 teams, ranking #4,5,6,7,8,9,10)

IV. Evaluation:

A: Evaluation method

The input for the LLM-based agent designed by participants is a natural language description, which could include the type of circuit to be designed and the corresponding design specifications. The agent must generate a corresponding SPICE netlist of an operational amplifier, which meets the given metrics listed in Table 1. The output netlist file of the agent should be named **AMP.cir**, which should include the designed circuit structure described in standard form and annotations explaining the internal submodules of the structure (in the form of comments).

To facilitate performance testing and standardized evaluation, the **AMP.cir** file must include a subcircuit definition encapsulating the operational amplifier (op-amp) circuit using the following SPICE command: **.SUBCKT AMP Vinp Vinn VDD VSS Vout**

The subcircuit name is fixed as **AMP**, and the port order must follow the example provided in the SPICE command. The op-amp subcircuit module is shown in Figure 1. Using a two-stage op-amp circuit as an example, an internal circuit diagram of the op-amp module is presented in Figure 2. For the competition, no specific number of stages or detailed structure is required for the op-amp; however, the overall architecture must support differential input and single-ended output.

During **the preliminary round**, the op-amp's bias current and voltage can be replaced with ideal current and voltage sources (e.g. the highlighted bias current sources of the two-stage op-amp circuit in Fig. 2).

During **the final round**, ideal sources for bias current and voltage are no longer allowed. Participants must design bias circuits implemented with transistors and include process corner simulations. Additionally, the runtime algorithm performance of the large-model agent will be evaluated (i.e. the time cost and memory cost of the LLM agent).

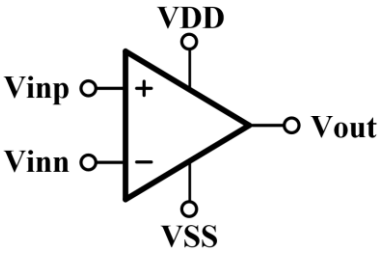

Figure 1. Op-amp subcircuit module diagram

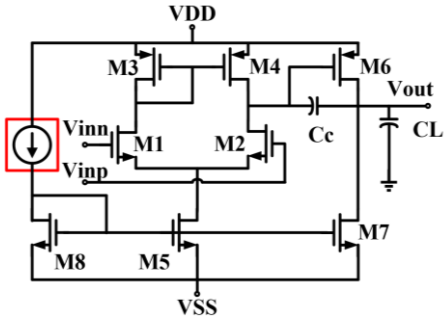

Figure 2. Example of an op-amp circuit structure

Notes:

1. The agent's tool invocation is limited to circuit simulation tools (**restricted to ngspice-43 version**). Conventional automated optimization algorithms are not allowed, and all component parameters in the netlist must be generated by the large model.

2. **All prompts used by the agent must be written in English** and **stored in a prompt folder as .txt files** for invocation. Participants are strictly prohibited from including pre-designed circuits in the prompts. Circuit examples may only include topologies without corresponding parameters. The organizing committee will inspect the submitted prompts for compliance.

3. The code for implementing agent must **be stored in an agent folder**, with each agent should be written in its own file and named in the format **[AgentName].py**. The testbench for invoking the agent to generate netlists should be in a file named **main.py**. The code submitted by participants must be clean, well-structured, and include comments explaining each section of the code.

4. The output netlist of the agent must maintain a certain level of stability. After the final round, the organizing committee will log into each team's server to verify reproducibility by the following two methods. **The scores of each team is considered to be valid if below validations test could be passed:**

   a) Given **10** validation opportunities, if the simulation results of the netlist generated by the agent have an error of less than 5% compared to the submitted netlist, it will be considered as passing this .

   b) The organizing committee will provide **five different design requirements** to the agent (identical for all teams and undisclosed in advance). Each requirement will target a single metric (e.g., GBW or SR). If the simulation result of the netlist generated by the agent for any one of the five requirements falls within the ±10% range of the given requirement, it will be considered as passing.

5. During the final round, participants must use Python with version 3.10.

6. The organizing committee reserves the final right to interpret the competition rules.

B: Scoring method

The competition consists of two stages: a preliminary round and a final round. Scores from the preliminary round will contribute proportionally to the final ranking. The operational amplifier (Op-Amp) is specified with a load capacitor CL=2 pF, VDD=1.8 V, and VSS=0 V. Participants in both the preliminary and final rounds are required to design circuits that meet the performance metrics for the op-amp. The final design metrics are evaluated using the circuit performance criteria shown in Table I. Performance scores of preliminary round are calculated by weighted average of the specification.

TABLE I. Performance Evaluation Criteria

Evaluation indicator	**Design requirements**
Open-loop gain **(Gain)**	> 60 dB
Gain Bandwidth **(GBW)**	> 20MHz

Phase Margin **(PM)**	> 60°
Slew Rate **(SR)**	> 20V/μS
Power consumption **(Idc)**	< 500μA

TABLE II. Scoring Criteria

Stage	Content	Scoring requirements
Preliminary	**Circuit Performance Metrics (82.5 points)**	**The evaluation includes five metrics, with each metric contributing 12 points. The remaining 22.5 points are assigned based on ranking of the participant's submission performance. Scores are calculated proportionally for metrics that do not meet requirements.**
	Algorithm Performance Metrics (7.5 points)	**Points are calculated based on the normalized total number of tokens in the submitted prompt files.**
	Documentation (10 points)	**Scored based on the structure and content of the submitted documentation.**
Final	**Circuit Performance Metrics (52.5 points)**	**The evaluation includes five metrics, with each metric contributing 6 points to meet the target. The remaining 22.5 points are assigned based on ranking of the participant's submission performance. Scores are calculated proportionally for metrics that do not meet requirements.**
	Circuit Additional Metrics (15 points)	**Includes metrics such as distortion and control ratio. Input noise is evaluated for each category, with scores calculated based on weightage and the performance of the submitted work.**
	Algorithm Performance Metrics (22.5 points)	**Points are calculated based on the normalized total number of tokens in the prompt files. The final prompt that meets the best requirements will receive the weighted evaluation.**
	Documentation (10 points)	**Scored based on the structure and content of the submitted documentation.**
	Note: Final scores are calculated as 80% of the Final Round score plus 20% of the Preliminary Round score to determine the overall ranking.	

Submission Requirements for the Preliminary Round:

During the preliminary round:

1. SPICE netlist file for the subcircuit: **AMP.cir**.
2. Simulation results for the performance metrics.
3. Performance script output file: **monitor_results.json** (token statistics results).

Within five days after the preliminary round ends:

1. **Technical Documentation:** A two-page document written in IEEE conference paper format, introducing the team's Agent framework and experimental results.
2. **Source Code:** The source code implementing the agent framework.
3. **Simulation Video:** A video demonstrating the SPICE netlist simulation, with a file size limit of 200 MB.

Submission Requirements for the Final Round:

During the final round:

1. SPICE netlist file for the subcircuit: **AMP.cir**.
2. Simulation results for the performance metrics.
3. Performance script output file: **monitor_results.json** (token statistics, timing, and memory test results)

Within ten days after the final round ends:

1. **Competition Paper:** A document should be written in IEEE conference paper format, detailing the team's Agent framework and experimental results.
2. **Source Code:** The complete source code for the Agent framework should be submitted. The competition organizers reserve the right to use the code and developed cases for promotional purposes in open-source communities (e.g., GitHub, Hugging Face) or within sponsor-related open-source tools.
3. **Simulation Video:** A video should be recorded for demonstrating the SPICE netlist simulation, with a file size limit of 200 MB.

A. Preliminary round evaluation:

1. Circuit Performance (Total: 82.5 Points)

Table I lists five specific evaluation parameters: **Gain**, **GBW**, **PM**, **SR**, and **Idc**. Each parameter contributes 12 points. For parameters other than **Idc**, if the target is not met, the score is calculated as the ratio of the actual value to the target value multiplied by

12. For Idc, if the target is not met, the score is calculated as the ratio of the target value to the actual value multiplied by 12.

The additional 22.5 points are assigned based on normalized weighting, with **Idc** having a weight of 2, **Gain**, **GBW**, and **SR** each having a weight of 1.5, and **PM** having a weight of 1, resulting in a total weight of 7.5. Thus, the maximum additional score for the first item is 6 points, for the next three items is 4.5 points, and for the last item is 3 points.

The highest and lowest values of the participant submissions are defined as $\mathbf{Gain_{max}}$, $\mathbf{GBW_{max}}$, $\mathbf{SR_{max}}$, $\mathbf{PM_{max}}$, $\mathbf{Idc_{max}}$, and $\mathbf{Gain_{min}}$, $\mathbf{GBW_{min}}$, $\mathbf{SR_{min}}$, $\mathbf{PM_{min}}$, $\mathbf{Idc_{min}}$, respectively. The formula for calculating the 22.5 additional points is as follows:

$$P_{Idc} = (1 - \frac{Idc - Idc_{min}}{Idc_{max} - Idc_{min}}) \times 6$$

$$P_{Gain} = \frac{Gain - Gain_{min}}{Gain_{max} - Gain_{min}} \times 4.5$$

$$P_{GBW} = \frac{GBW - GBW_{min}}{GBW_{max} - GBW_{min}} \times 4.5$$

$$P_{SR} = \frac{SR - SR_{min}}{SR_{max} - SR_{min}} \times 4.5$$

$$P_{PM} = \frac{PM - PM_{min}}{PM_{max} - PM_{min}} \times 3$$

2. Algorithm Performance Metrics (Total: 7.5 points)

The organizing committee will evaluate the prompt files submitted by participants based on counting the total **token** number. Scores are normalized and weighted, with lower token usage corresponding to higher scores. The maximum and minimum token amount from the submissions are denoted as $\mathbf{Token_{max}}$ and $\mathbf{Token_{min}}$, respectively. The scoring formula for the 7.5 points is as follows:

$$P_{Token} = (1 - \frac{Token - Token_{min}}{Token_{max} - Token_{min}}) \times 7.5$$

3. Document Writing (Total: 10 Points)

Scores are awarded based on the structure and content of the submitted documentation. The document should have a standardized structure and clear content.

B. Final round evaluation:

1. Circuit Performance (Total: 52.5 Points)

Table I lists five performance evaluation specifications: **Gain**, **GBW**, **PM**, **SR**, and **Idc**. Each specification contributes 6 points. For the final round, participants must complete process corner simulations **(TT, FF, SS, SF, FS)** for the five parameters, with **the minimum value used as the result**. For parameters other than **Idc**, if the target is not met, the score is calculated as the ratio of the actual value to the target value multiplied by 6. For Idc, if the target is not met, the score is calculated as the ratio of the target value to the actual value multiplied by 6.

The additional 22.5 points are assigned based on normalized weighting, with **Idc** having a weight of 2, **Gain**, **GBW**, and **SR** each having a weight of 1.5, and **PM** having a weight of 1, resulting in a total weight of 7.5. Thus, the maximum additional score for the first item is 6 points, for the next three items is 4.5 points each, and for the last item is 3 points.

The highest and lowest values of the participant submissions are defined as $\mathbf{Gain_{max}}$, $\mathbf{GBW_{max}}$, $\mathbf{SR_{max}}$, $\mathbf{PM_{max}}$, $\mathbf{Idc_{max}}$, and $\mathbf{Gain_{min}}$, $\mathbf{GBW_{min}}$, $\mathbf{SR_{min}}$, $\mathbf{PM_{min}}$, $\mathbf{Idc_{min}}$, respectively. The formula for calculating the 22.5 additional points is as follows:

$$P_{Idc} = (1 - \frac{Idc - Idc_{min}}{Idc_{max} - Idc_{min}}) \times 6$$

$$P_{Gain} = \frac{Gain - Gain_{min}}{Gain_{max} - Gain_{min}} \times 4.5$$

$$P_{GBW} = \frac{GBW - GBW_{min}}{GBW_{max} - GBW_{min}} \times 4.5$$

$$P_{SR} = \frac{SR - SR_{min}}{SR_{max} - SR_{min}} \times 4.5$$

$$P_{PM} = \frac{PM - PM_{min}}{PM_{max} - PM_{min}} \times 3$$

2. Additional Circuit Indicators (Total: 15 Points)

Common-mode rejection ratio (**CMRR**), power supply rejection ratio (**PSRR**), and **equivalent input noise voltage** (**NOISE**) at **1 kHz** each contribute 5 points. The minimum and maximum values of the submissions are defined as $\mathbf{CMRR_{min}}$, $\mathbf{PSRR_{min}}$, $\mathbf{NOISE_{min}}$, and $\mathbf{CMRR_{max}}$, $\mathbf{PSRR_{max}}$, $\mathbf{NOISE_{max}}$, respectively. The formula for

calculating the scores is as follows:

$$P_{CMRR} = \frac{CMRR - CMRR_{min}}{CMRR_{max} - CMRR_{min}} \times 5$$

$$P_{PSRR} = \frac{PSRR - PSRR_{min}}{PSRR_{max} - PSRR_{min}} \times 5$$

$$P_{NOISE} = (1 - \frac{NOISE - NOISE_{min}}{NOISE_{max} - NOISE_{min}}) \times 5$$

3. Algorithm Performance (Total: 22.5 Points)

Token amount, runtime (**TIME**) and memory resource cost (**RU**) contribute 7.5 points respectively. The maximum and minimum token amount, shortest and longest runtime cost, and minimum and maximum memory cost are defined as **Token$_{max}$**, **Token$_{min}$**, **TIME$_{min}$**, **TIME$_{max}$**, **RU$_{min}$**, and **RU$_{max}$**, respectively. The formulas for calculating the scores are as follows:

$$P_{Token} = (1 - \frac{Token - Token_{min}}{Token_{max} - Token_{min}}) \times 7.5$$

$$P_{TIME} = (1 - \frac{TIME - TIME_{min}}{TIME_{max} - TIME_{min}}) \times 7.5$$

$$P_{RU} = (1 - \frac{RU - RU_{min}}{RU_{max} - RU_{min}}) \times 7.5$$

4. Document Writing (Total: 10 Points)

Scores are based on the structure and content of the submitted documentation. The document should have a standardized structure and clear content.

Notes:

1. The **transistors** should utilize the models specified in the **Skywater130 process**, and resistors and capacitors can adopt ideal models.
2. The input common-mode voltage **Vcm** should be set to **VDD/2 (0.9V)** and applied during AC, DC, and noise simulations.
3. For the simulation of **slew rate (SR)**, the output voltage range is selected from **10% (0.18V) to 90% (1.62V)** of the rising edge amplitude. The input signals are a pulse voltage ranging from 0 to VDD applied at the non-inverting input node and a pulse voltage ranging from VDD to 0 applied at the inverting input

node.

4. **Power consumption (Idc)** refers to the output current of the external voltage source VDD (including the operational amplifier and the bias circuit's operating current).
5. **Equivalent input noise voltage (NOISE)** should be simulated in V/√Hz.
6. Both **CMRR** and **PSRR** should be simulated at 1 Hz.

V. Committee:

- Xidian University: Wei Mao, Bo Li
- Shanghai Jiao Tong University: Yongfu Li, Zhezhi He
- Nanjing University: Li Du, Yuan Du
- University of Electronic Science and Technology of China: Liang Chang
- T-head (Shanghai) Semiconductor Technology Co., Ltd.: Xiaohan Ma, Guosheng Yu
- Arm Technology (China) Co., Ltd.: Fengzhi Pan, Xile Yang

VI. Relevant Links:

- 2025 AICAS: http://www.aicas2025.org/
- T-Head Semiconductor Co., Ltd.: https://www.t-head.cn/
- Tongyi Qianwen: https://qianwen.aliyun.com/
- Arm Technology (China): https://www.armchina.com/
- Hugging Face (Download link for Qwen models globally): https://huggingface.co/Qwen
- ModelScope (Download link for Qwen models in Chinese):
- https://www.modelscope.cn/organization/Qwen
- Qwen Documentation: https://qwen.readthedocs.io/zh-cn/latest/getting_started/quickstart.html
- IEEE Conference Paper Template: https://template-selector.ieee.org/secure/templateSelector/publicationType
- SkyWater PDK: https://skywater-pdk.readthedocs.io/en/main/